In the Claims:

1.-30. (Cancelled)

31. (Currently Amended) An automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

(1) determining a critical path length (C) of the layout portion;

(2) determining a minimum path length (MPL) for every path within the layout;

(3) unlocking all branches of the layout;

(4) determining any branches of the paths in the layout where the minimum path length (MPL) for that path is equal to the critical path length (C) and locking those branches of the layout;

(5) determining whether any branches of the layout remain unlocked, if no branches remain unlocked then the method is complete;

(6) determining which of the unlocked branches of the layout has the smallest actual spacing and designating that branch as the branch (K) for processing;

(7) determining the width of the spacing between the neighbor branches on either side of branch (K);

(8) determining whether the actual spacing of the branch (K) plus a predetermined incremental spacing amount is less than or equal to the larger of the spacing of that unlocked branch that is the predecessor branch and less than or equal to the spacing of the unlocked branch that is the successor branch, and if the spacing of the particular branch (K) plus the predetermined incremental spacing amount is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch (K) and returning to

the step (5);

(9) determining whether the graph connectivity restrictions of the layout allow the spacing of the particular branch (K) to be increased by the predetermined incremental spacing, if the graph connectivity restrictions of the layout does not allow the spacing for the particular branch (K) to be increased, locking the particular branch and returning to the step (5);

(10) increasing the spacing of the particular branch (K) by the predetermined incremental spacing amount;

(11) updating the graph connectivity of the layout; and

(12) returning to step (5).

32. (Previously Presented) The method of Claim 31, and further comprising:

(13) subsequent to performing step (10) and prior to performing step(11), decreasing the spacing of the larger of the predecessor branch and the successor branch to the branch (K) by the predetermined incremental spacing.

33. (Previously Presented) The method of Claim 31, wherein the critical path length (C) represents a dimensional constraining below which the layout portion cannot be reduced in size in a particular direction.

34. (Previously Presented) The method of Claim 31, wherein the minimum path length (MPL) represents the smallest path length in which the features and the spacing of a particular path can be disposed while still preserving connectivity to other paths in the layout.

35. (Currently Amended) A machine-readable medium having recorded on it a set of instructions for performing an automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

(1) determining a critical path length (C) of the layout portion;

(2) determining a minimum path length (MPL) for every path within the layout;

(3) unlocking all branches of the layout;

(4) determining any branches of the paths in the layout where the minimum path length (MPL) for that path is equal to the critical path length (C) and locking those branches of the layout;

(5) determining whether any branches of the layout remain unlocked, if no paths remain unlocked then the method is complete;

(6) determining which of the unlocked branches of the layout has the smallest actual spacing and designating that branch as the branch (K) for processing;

(7) determining the width of the spacing between the neighbor branches on either side of branch (K);

(8) determining whether the actual spacing of the branch (K) plus a predetermined incremental spacing amount is less than or equal to the larger of the spacing of the unlocked branch that is the predecessor branch and to the spacing of the unlocked path that is the successor branch, and if the spacing of the particular branch (K) plus the predetermined incremental spacing amount is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch (K) and returning to the step (5);

(9) determining whether the graph connectivity restrictions of the layout allow the spacing of the particular branch (K) to be increased by the predetermined incremental spacing

amount, if the graph connectivity restrictions of the layout does not allow the spacing for the particular branch (K) to be increased, locking the particular branch (K) and returning to the step (5);

(10) increasing the spacing of the particular branch (K) by the predetermined incremental spacing amount;

(11) updating the graph connectivity of the layout; and

(12) returning to step (5).

36. (Currently Amended) The machine readable medium of Claim 35, and further comprising:

(13) subsequent to performing step (10) and prior to performing step (11), decreasing the spacing of the larger of the predecessor branch and the successor branch to the branch (K) by the predetermined incremental spacing amount.

37. (Previously Presented) The machine readable medium of Claim 35, wherein the critical path length (C) represents a dimensional constraining below which the layout portion cannot be reduced in size in a particular direction.

38. (Previously Presented) The machine-readable medium of Claim 35, wherein the minimum path length (MPL) represents the smallest path length in which the features and the spacing of a particular path can be disposed while still preserving connectivity to other paths in the layout.

39. (Currently Amended) A system operable to de-compact a layout for a portion of an integrated circuit, said system comprising a processor specially adapted to perform an automatic machine implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

(1) determining a critical path length (C) of the layout portion;

(2) determining a minimum path length (MPL) for every path within the layout portion;

(3) unlocking all branches of the layout portion;

(4) determining any branches of the paths in the layout portion where the minimum path length (MPL) for that path is equal to the critical path length (C), and locking those branches of the layout;

(5) determining whether any branches of the layout remain unlocked, if no branches remain unlocked then the method is complete;

(6) determining which of the unlocked branches of the layout has the smallest actual spacing and designating that branch as the branch (K) for processing;

(7) determining the width of the spacing between the neighbor branches on either side of branch (K);

(8) determining whether the actual spacing of the branch (K) plus a predetermined incremental spacing amount is less than or equal to the larger of the spacing of that unlocked branch that is the predecessor branch and less than or equal to the spacing of the unlocked branch that is the successor branch, and if the spacing of the particular branch (K) plus the predetermined incremental spacing amount is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch (K) and returning to the step (5);

(9) determining whether the graph connectivity restrictions of the layout allow the spacing of the particular branch (K) to be increased by the predetermined incremental spacing amount, if the graph connectivity restrictions of the layout does not allow the spacing for the particular branch (K) to be increased by the predetermined incremental spacing amount, locking the particular branch (K) and returning to step (5);

(10) increasing the spacing of the particular branch (K) by the predetermined incremental spacing amount;

(11) updating the graph connectivity of the layout; and

(12) returning to step (5).

40. (Currently Amended) The system of Claim 39, and further comprising:

(13 ) subsequent to performing step (10) and prior to performing step (11), decreasing the spacing of the larger of the predecessor branch and the successor branch to the branch (K) by the predetermined incremental spacing amount.

41. (Previously Presented) The system of Claim 39, wherein the critical path length (C) represents a dimensional constraining below which the layout portion cannot be reduced in size in a particular direction.

42. (Previously Presented) The system of Claim 39, wherein the minimum path length (MPL) represents the smallest path length in which the features and the spacing of a particular path can be disposed while still preserving connectivity to other paths in the layout.